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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,972	12/03/2003	Jock F. Tomlinson	L00-010C1	5095

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EXAMINER	
SURYAWANSHI, SURESH	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 03/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,972	TOMLINSON ET AL.	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-15 and 25-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-15 and 25-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6, 8-15 and 25-34 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 8, 10-13, 25-29 and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henze (US Patent 5,821,755[1]) in view of Borza (US Patent 6,430,444).

4. As per claim 1, Henze discloses a power management integrated circuit comprising:

a plurality of input terminals adapted to receive analog input voltage signals [Fig. 1; col. 3, lines 56-59; input terminals 14A and 14B];

a plurality of analog input monitor circuits coupled to the input terminals, each analog input monitor circuit operable to compare an input analog voltage received at an input terminal against at least one voltage reference [Fig. 1; col. 3, line 56 -- col. 4, line 8; comparators 46 and 48 and a voltage reference generator 52];

control logic coupled to the plurality of analog input monitor circuits and operable to generate at least one control signal in response to output signals from the analog input monitor circuits [Fig. 1; col. 4, lines 4-8; a control logic (flip-flop 60) outputs a control signal 62 in response to output signals from the comparators 46 and 48]; and

at least one driver circuit coupled between the control logic and an output terminal and capable of controlling a power switch, the drive circuit operable in response to a control signal from the control logic [Fig. 1; col. 4, lines 18-30; a power switch driver 64 controls the switching device 16 in response to the control signal 62 from the control logic 60].

Henze does not disclose using FET driver circuit. But a routineer in the art would know about a FET driver circuit as it is well known for switching transistors in a programmable power control circuit. However, Borza clearly discloses a programmable power control circuit to generate a ramp control signal that gradually turns on a FET drive circuit [Fig. 2, 4, 5; col. 4, lines 55-60; col. 5, lines 15-30; col. 6, line 63 -- col. 7, line 12]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to power control of a device. Moreover, Henze's device will clearly be benefited with the improved design of Borza because of the use of a programmable logic and FET drivers.

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[1] The prior art cited by the examiner in the prior office action.

5. As per claims 27 and 31, Henze discloses a power management integrated circuit as detailed above. Henze discloses the invention utilizing a flip-flop and power switch driver. Henze does not expressly disclose that the power switch driver could have been a FET driver and the flip-flop could be replaced with a FPGA. But a routineer in the art would know about a FET driver and a FPGA as these are well known for their use in the art. However, Borza clearly discloses a programmable power control circuit to generate a ramp control signal that gradually turns on a FET drive circuit [Fig. 2, 4, 5; col. 4, lines 55-60; col. 5, lines 15-30; col. 6, line 63 -- col. 7, line 12]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to power control of a device. Moreover, Henze's device will clearly be benefited with the improved design of Borza because of the use of a programmable logic and FET drivers.

6. As per claim 2, Henze discloses that at least one analog input monitor circuit is operable to compare an input analog voltage against high and low voltage reference [Fig. 1; voltage reference generator 52].

7. As per claim 3, Henze discloses that at least one analog input monitor circuit is operable to compare a first input analog voltage received at a first input terminal to a second input analog voltage received at a second input terminal [Fig. 1; comparators 46 and 48].

8. As per claim 4, Henze discloses that at least one analog input monitor circuit is operable to monitor the voltage across an external resistor, and the control logic is operable to generate an indicator signal in response to the output signal from the analog input monitor circuit [Fig. 1; col. 4, lines 4-8; a control logic (flip-flop 60) outputs a control signal 62 in response to output signals from the comparators 46 and 48].

9. As per claim 5, Henze discloses that a programmable voltage reference generator [Fig. 1; voltage reference generator 52].

10. As per claim 6, Borza discloses a plurality of FET driver circuits, wherein the control logic is programmable to generate a plurality of respective ramp control signals to turn on the FET driver circuits in a programmable sequence [Fig. 2, 4, 5; col. 4, lines 55-60; col. 5, lines 15-30; col. 6, line 63 -- col. 7, line 12].

11. As per claim 8, Borza discloses that the control logic is programmable [Fig. 2, 4, 5; col. 4, lines 55-60; col. 5, lines 15-30; col. 6, line 63 -- col. 7, line 12].

12. As per claims 10 and 33, Borza discloses that the FET driver circuit is programmable [Fig. 2, 4, 5; col. 4, lines 55-60; col. 5, lines 15-30; col. 6, line 63 -- col. 7, line 12].

13. As per claim 11, Borza discloses that a charge pump circuit coupled to the driver circuit [inherent to a system having a driver circuit].

14. As per claim 12, Borza discloses that the FET driver circuit comprises an FET driver circuit capable of driving a power MOSFET switch coupled to the output terminal [Fig. 2, 4, 5; col. 4, lines 55-60; col. 5, lines 15-30; col. 6, line 63 -- col. 7, line 12].

15. As per claim 13, Henze discloses that a serial interface coupled to the control logic [inherent to the system as the control logic is connected to a power switch driver].

16. As per claims 25, 29 and 32, Borza discloses that the control logic is operable to provide a plurality of selectable ramp control signals that vary in the rate at which they turn on the FET driver circuit [Fig. 2, 4, 5; col. 4, lines 55-60; col. 5, lines 15-30; col. 6, line 63 -- col. 7, line 12; inherent to the system].

17. As per claim 26, Borza discloses that that the ramp control signal is generally monotonic and linear [Fig. 2, 4, 5; col. 4, lines 55-60; col. 5, lines 15-30; col. 6, line 63 -- col. 7, line 12; inherent to the system].

18. As per claim 28, Borza discloses that the control logic is programmable [Fig. 2, 4, 5; col. 4, lines 55-60; col. 5, lines 15-30; col. 6, line 63 -- col. 7, line 12].

19. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Henze (US Patent 5,821,755[1]), Borza (US Patent 6,430,444) in view of Sharpe-Geisler et al (US Patent 5,751,164[1]; hereinafter Sharpe).

20. As per claim 9, Henze and Borza disclose the invention substantially. Henze and Borza do not disclose about the control logic including a plurality of macrocells. However, Sharpe clearly discloses that use of macrocells in a complex programmable logic device is common [col. 2, lines 44-65] and a routineer in the art would know that a function as complex as a flip-flop can be implemented. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are related to power control of a device.

21. Claims 14, 30 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henze (US Patent 5,821,755[1]), Borza (US Patent 6,430,444) in view of Kunz et al (US Patent 6,701,442[1]; hereinafter Kunz).

22. As per claims 14, 30 and 34, Henze and Borza disclose the invention substantially. Henze and Borza do not expressly disclose about a nonvolatile programmable memory. But a routineer in the art would know that it is common to have a memory to store power management configuration information or indication in a computer system to control the power. However, Kunz clearly discloses such a nonvolatile memory for storing power configuration [Fig 2, 3; NV Memory 150; col. 6, lines 18-24; col. 8, lines 13-16]. Therefore, it would have been obvious to

one of ordinary skill in the art at the time the invention was made to combine the cited references as they are related to power control and management in a computer system.

23. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Henze (US Patent 5,821,755[1]), Borza (US Patent 6,430,444) in view of Little (US Patent 5,175,845).

24. As per claim 15, Henze and Borza disclose the invention substantially. Henze and Borza do not disclose about a watchdog timer coupled to the control logic. However, Little clearly discloses that a watchdog timer is well known in the art and it is used to force a circuit into a reset state [col. 6, lines 3-10; col. 14, lines 16-30]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are related to power control and management in a computer system. Moreover, a watchdog timer will enhance the power management circuit of Henze, as now there will be a timer to reset the circuit if the circuit does not respond in a predetermined time period. Thus, one can avoid the system hanging for an unknown period of time.

Response to Arguments

25. Applicant's arguments with respect to claims 1-6, 8-15 and 25-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
March 22, 2006